

Features

- Transceiver unit with independent
 - 1310nm DFB diode transmitter
 - APD receiver
- Multi-sourced 2×10 package style with duplex LC receptacle
- Metal enclosure for lower EMI
- +3.3V Single power supply
- Operating temperature: 0~70°C
- Operates data rates from 5Mb/s to 1270Mb/s (NRZ)
- Qualified to meet the intent of Bellcore 468 reliability practices
- LVPECL logic interface simplifiers interface to external circuitry
- LVTTTL logic signal detect output
- SONET OC-24 and IEEE 802.3Z Gigabit Ethernet applications

Application

- SONET/SDH
- ATM

General

The optical transceiver is a high performance, cost effective module for serial optical data communication application.

Transmitter Section

Transmitter is designed for single mode fiber and operates at a nominal wavelength of 1310nm. The transmitter module uses a DFB laser diode and full IEC 825 and CDRH class 1 eye safety. It contains APC function, temperature compensation circuit to ensure the module meet ITU-TG.957 requirement at operating temperature, LVPECL data inputs and AC coupling circuit. The module provides LVTTTL Tdis input interface, LD bias current bias monitor and output optical power monitor as shown in figure1.

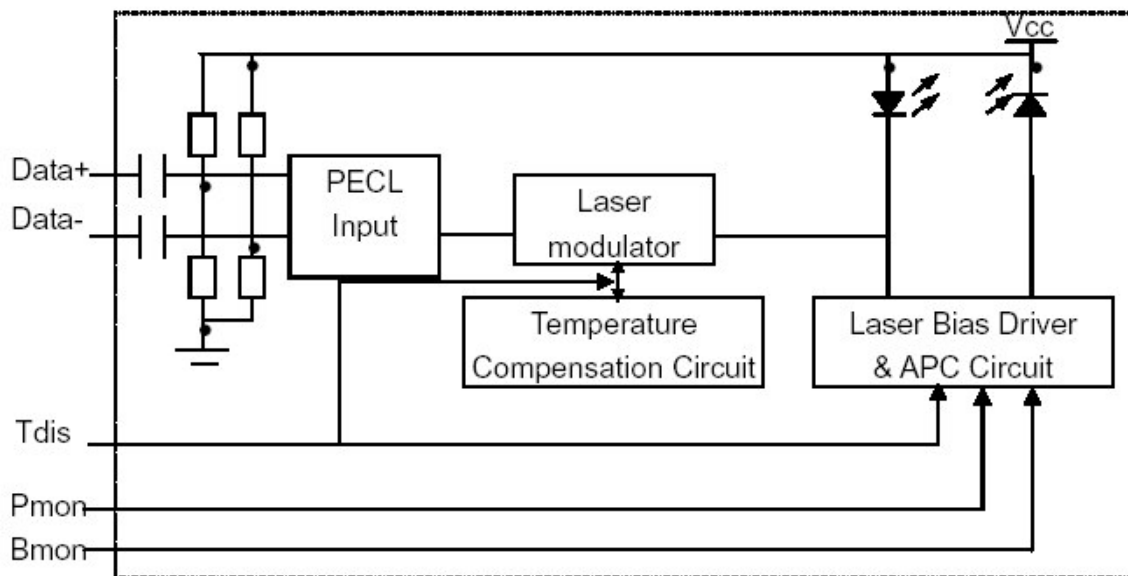


Figure1. Transmitter Block Diagram

Transmitter Power Disable Section

The output power can be disabled via the single TDis pin. Logic 1 disables the transmitter. This pin is internally pulled low, and hence if left unconnected this pin will beat logic level 0 and the module will operate normally.

Laser Bias Monitor

The laser bias monitor proportion with the bias current, the analog current is monitored by measuring the voltage drop across a 10 ohm resistor, the monitor circuit block diagram is shown in figure 2.

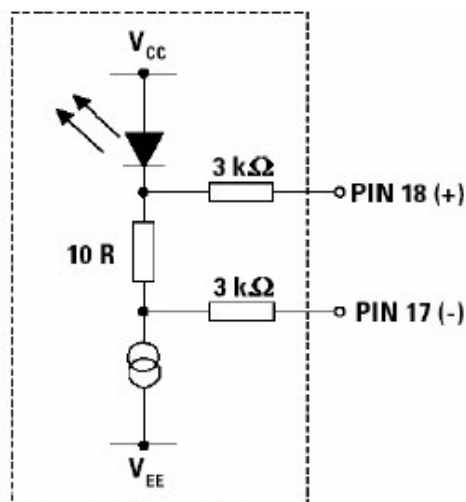


Figure2 LD Bias Current Monitor Circuit

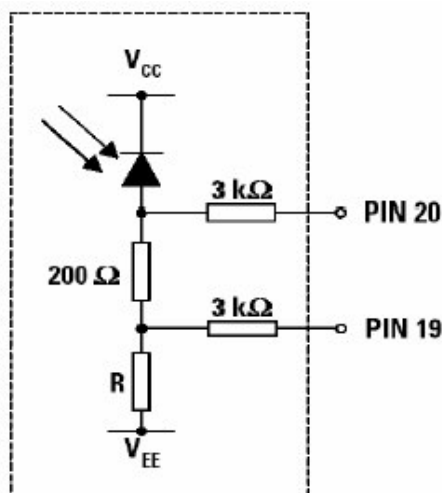


Figure 3 Power Monitor Circuit

Transmitter Power Monitor

The transmitter power monitor proportion with the transmitter power. The analog voltage measured at 10km ohm resistor that the rear optical current through. The block diagram as figure 3

Receiver Section

The receiver section uses a hermetic packaged APDTIA (APD and trans-impedence amplifier) and a limiting amplifier. Which transforms input optical power to optical current through APD. And the optical current is transformed to voltage signal by trans-impedence amplifier. Differential DATA and /DATA LVPECL data signal that is AC output is produced by limiting amplifier and voltage signal that is through limiting amplifier and filter. The receiver signal detected monitors input optical signal. When the optical power is not enough to support module operating normally, SD pin will beat LVTTTL logic level 0 and signal detect appears. The APDTIA is ac coupled to preamplifier through a low pass filter, as shown in figure 4. The capacitor and LPF are enough to pass the signal from 5Mb/s TO 1270Mb/s without significant distortion or performance penalty.

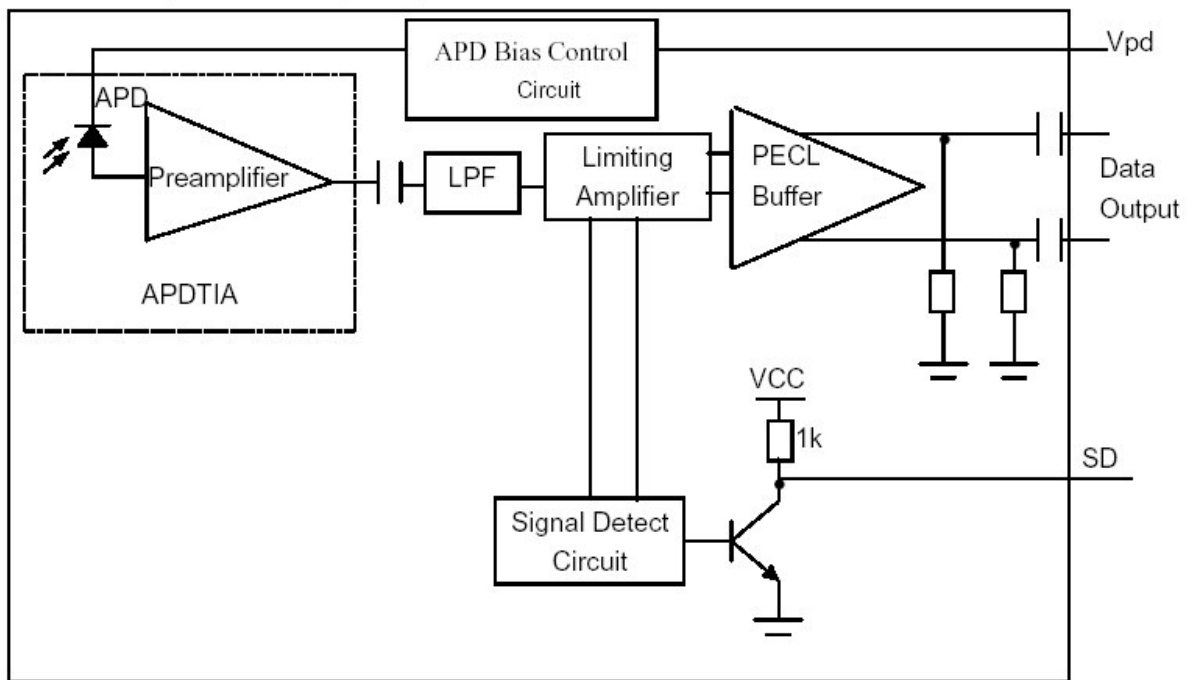


Figure 4. Receiver Block Diagram

Performance Specifications

Table1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tst	-40	+85	°C
Input Voltage	-	GND	Vcc	V
Power Supply Voltage	Vcc-Vee	-0.5	+3.6	V
Lead Soldering Temperature/Time	-	-	260/10	°C/S
Operating Temperature	To	0	+70	°C

Note: Stress in excess of maximum absolute ratings can cause permanent damage to the module

Tabel 2. Operating Environment

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	+3.1	+3.5	V
Ambient Operating Temperature		0	+70	°C

Tabel 3. Optical and Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Center Wavelength	λ_p	1280	1310	1335	nm	
Spectral Width	$\Delta\lambda$	-	-	1	nm	
Side Mode Suppression Ratio	SMRS	30	-	-	dB	
Average Optical Output Power	Po	-2	-	+3	dBm	
Extinction Ratio	Er	8.2	-	-	dB	
Input signal Amplitude	Vpp	300	-	1600	mV	
Power Supply Current	ICC	-	90	180	mA	1
Laser Bias Monitor (Lmon(+)-Lmon(-))		0.01	-	0.9	V	
Power Monitor (Pmon(+)-Pmon(-))	-	0.01	-	0.2	V	
Transmitter Disable Voltage	VD	2.0	-	Vcc		
Transmitter Enable Voltage	VEN	0	-	0.8	V	
Receiver Specifications						
Parameter	Symbol	Min	Typ	Max	Unit	Note
Operate wavelength	λ	1260		1580	nm	
Sensitivity	Pr	-	-30	-28	dBm	2
Maximum input power	Ps	-9	-	-	dBm	2
Signal Detect Assert Level	-	-	-	-28	dBm	Low Level: Alarm
Signal Detect Deassert Level	-	-45	-	-	dBm	
Signal Detect Hysteresis		-	1	4	dB	
SD LOW-level output voltage	VLout	-	-	0.8	V	
SD HIGH-level output voltage	VHout	2.0	-	-	V	
Power Supply Current	Icc	-	110	180	mA	1
Output Data Amplitude	Vpp	400	500	2000	mV	

Note :

- The current excludes the output load current.**
- Minimum sensitivity and saturation levels for a $2^{23} - 1$ PRBS with 72 ones and 72 zeros inserted (ITU recommendation G958)**
- RL=50R connected to a level of Vcc -2V.**

Pin Definitions

Pin Out Diagram

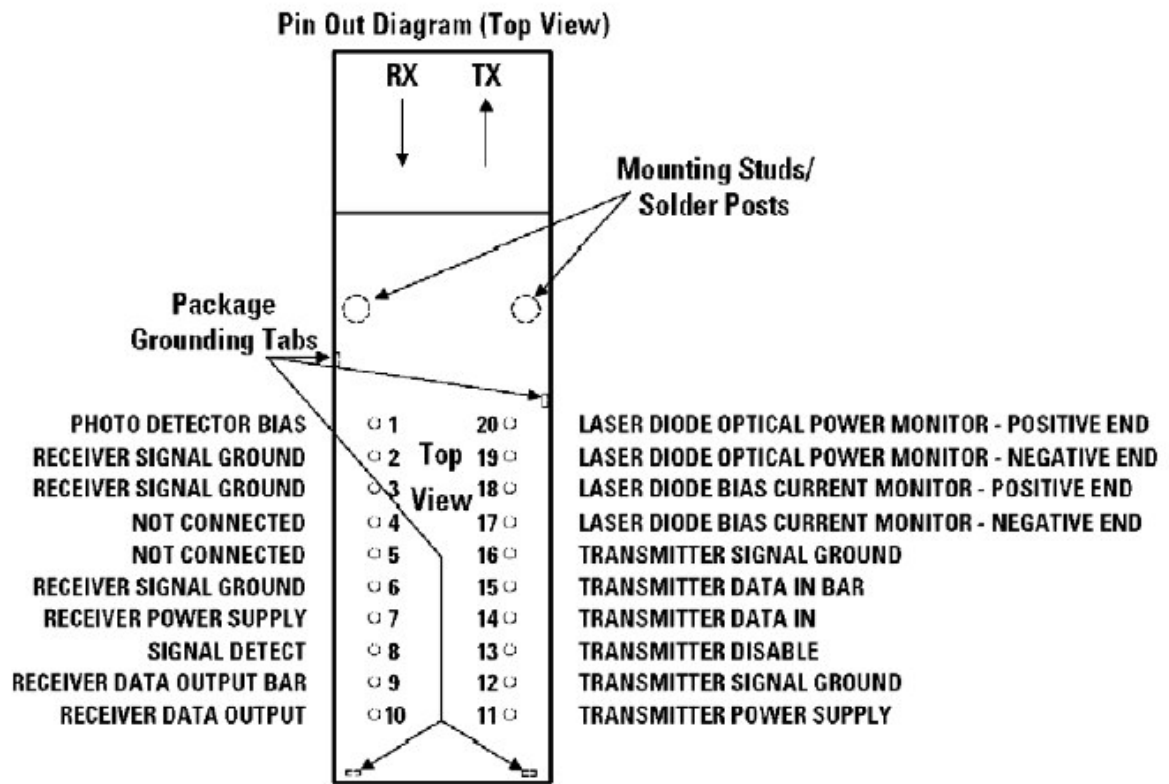


Figure 5. Pin Out Diagram

Pin Description

Pin#	Name	Function	Note
		Mounting Studs/Solder Poster	Note 1
		Package Grounding Tabs	Note 2
1	Vpd	Photon detector Bias	Note 3
2	VEER	Receiver Signal Grounding	Note 4
3	VEER	Receiver Signal Grounding	Note 4
4	NC	Not Connected	
5	NC	Not Connected	
6	VEER	Receiver Signal Grounding	Note 4
7	VCCR	Receiver Power Supply	Note 5
8	SD	Signal Detect	Note 6
9	RD-	Receiver Data Out Bar	PECL logic family. DC coupled
10	RD+	Receiver Data Out	PECL logic family. DC coupled
11	VCCT	Transmitter Power Supply	Note 7
12	VEET	Transmitter Signal Ground	Note 8
13	TxDis	Transmitter Disable	Note 9
14	TD+	Transmitter Data In	PECL logic family
15	TD-	Transmitter Data In Bar	PECL logic family
16	VEET	Transmitter Signal Ground	Note 8
17	BMON-	Laser Diode Bias Current Monitor-	Note 10
18	BMON+	Laser Diode Bias Current Monitor+	Note 10
19	PMON-	Rear Facet Monitor-	Note 11
20	PMON+	Rear Facet Monitor+	Note 11

Note:

1. **The two mounting studs did not be connected to the interior of ground. They are provided for transceiver mechanical attachment to the circuit board. It is recommended that the holes in the circuit board be connected to chassis ground.**
2. **Those tabs did not be connected to the interior of ground. Connect four package grounding tabs to receiver signal ground.**
3. **This pin enables monitoring of photo detector bias current. The pin should either be connected directly to VCCR_X, or to VCCR_X through a resistor for monitoring photo detector bias current.**
4. **Directly connect these pins to the receiver ground plane.**
5. **Provide +3.3V DC via the recommend receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the VCCR_X pin.**
6. **Normal optical input levels to the receiver result in logic "1" output. Low optical input levels to the receiver result in a logic "0" output.**
7. **Provide +3.3V DC via the recommended transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the VCCR TX pin.**
8. **Directly connect these pins to the transmitter signal ground plane.**
9. **LVTTL logic lever, to enable module connect to TTL logic low "0".**

- 10. The laser diode bias current is accessible by measuring the voltage developed across pins 17 and 18.
- 11. The rear facet monitor is accessible by measuring the voltage developed across pins 19 and 20.

Package Information

Unit: mm

